REMARKS

In view of the comments below, Applicant respectfully requests that the Examiner reconsider the present application including rejected claims 1-24, and withdraw the pending rejections.

Priority

The applicant notes with appreciation the acknowledgement of the claim for priority under 35 U.S.C. § 119 and the acknowledgement of receipt of papers submitted under 35 U.S.C. § 119(a)-(d).

Claim Objections

The Examiner has objected to claim 22 based on an informality. In particular, the Examiner notes that line 7 ends with a period in the middle of the claim.

By this response, Applicants have amended claim 22, line 7 to replace the period with a semicolon. In addition, Applicants have deleted the word "and" at the end of claim 22, line 5. These amendments should eliminate any informality from claim 22.

This amendment is being made solely to correct formal matter, and not in response to an art rejection. Any narrowing amendment to the claims in the present amendment is not to be construed as a surrender of any subject matter between the original claims and the present claims; rather this is merely an attempt at providing one or more definitions of what the applicant believes to be suitable patent protection. The present claims provide the intended scope of protection that the applicant is seeking for this application. Therefore, no estoppel

should be presumed, and the applicant's claims are intended to include a scope of protection under the Doctrine of Equivalents.

Based on at least the above amendment, Applicants submit that claim 22 has no remaining informalities. Applicants therefore respectfully request that the Examiner withdraw the objection of claim 22.

Claim Rejections 35 USC § 102

The Examiner has rejected claims 1-5, 7, 9-14, 16, and 18-24 under 35 U.S.C. § 102(b) as being allegedly anticipated by WIPO publication WO 02/09331 A2 by Lockridge et al. ("Lockridge").

Applicants respectfully traverse this rejection. However, in an effort to expedite prosecution, Applicants have amended independent claims 1, 10, 19, and 22 to better recite the present invention.

In particular, Applicants have amended claims 1 and 10 to recite "sequentially detecting a plurality of global synchronizing events, each of the plurality of global synchronizing events being associated with one of a plurality of different global synchronizing event identifiers," and that the recited time stamp information "is identified relative to one of the plurality of different global synchronizing event identifiers associated with one of the plurality of global synchronizing events." Support for these amendments can be found, for example, in paragraphs 0019, 0023, 0029, 0030, 0037, 0039, 0047, 0048, 0056, 0058, 0063, 0106, and 0113 of Applicants' specification.

These amendments make it clear that the global synchronizing events are not simply periodic events that provide a generic timing reference for synchronizing a clock. Rather,

they are events that are each identified by a different global synchronizing event identifier (e.g., a unique beacon number). And the recited time stamp is identified relative to one of these different global synchronizing event identifiers.

The Examiner relies upon the System Clock Recovery (SCR) information in Lockridge as allegedly showing the recited global synchronizing events. However, Lockridge simply discloses that transport packets can include SCR information that are used by a receiver to frequency lock its local clock to a head end system clock, to manage buffer levels, and to derive video timing and color burst signals in an integrated receiver decoder. (See, e.g., Locklear, page 5, lines 15-22, and FIG. 2.) There is nothing in Lockridge that discloses that each transmission of SCR information be associated with a different identifier, as would be required by amended claims 1 and 10.

In addition, nothing in Lockridge discloses that time stamp information is identified relative to one of a plurality of different global synchronizing event identifiers associated with one of the plurality of global synchronizing events. The Examiner relies upon the time stamps T1 in Lockridge as allegedly showing this feature. In particular, he asserts that since the server in Lockridge is frequency locked to the head end, the system time stamp T1 is a time stamp that ensures that any client device may reproduce the arrival time, even if the global synchronizing event itself is not forwarded to it. Thus, the Examiner appears to say that even if a client 204 in Lockridge doesn't receive a global synchronizing event, its client system clock will be frequency locked with a server system clock, which is itself synchronized to the global synchronizing event.

But amended claims 1 and 10 specifically require that the time stamp information be identified with respect to one of a plurality of different global synchronizing event

identifiers. And neither the system time stamps T1 in Lockridge, nor any other time stamp in Lockridge disclose such a feature. Simply being frequency locked with an SCR does not meet this limitation.

Applicants have also amended claim 19 to recite "a detection circuit for detecting a global synchronizing event, the global synchronizing events being associated with one of a plurality of different global synchronizing event identifiers, and receiving a second free-running timing value from the series of increasing free-running timing values," and "a wireless transceiver for adding the second free-running timing value and the one of the plurality of different global synchronizing event identifiers associated with the global synchronizing event to the host interface packet to form an air link frame, and transmitting the air link frame over a wireless channel to a remote wireless device." Lockridge fails to show this feature for reasons comparable to those given above for claims 1 and 10.

In particular, nothing in Lockridge discloses adding one of a plurality of different global synchronizing event identifiers associated with a global synchronizing event to a host interface packet to form an air link frame, as would be required by amended claim 19. As noted above, the SCRs do not have different global synchronizing event identifiers associated with each of them.

In addition, claim 22 recites a receiver device for receiving host data over a wireless channel, comprising: a free-running timer for providing a series of increasing free-running timing values; a detection circuit for detecting a global synchronizing event and receiving a free-running timing value from the series of increasing free-running timing values; a wireless transceiver for receiving an air link frame having a host interface packet and a first time stamp, the host interface packet including a second time stamp; a first time stamp processor

for receiving the first time stamp and comparing the first time stamp with a recorded free-running timing value to determine a timer correction value for the receiver device; a second time stamp processor for receiving the second time stamp and generating a host data process signal based on the second time stamp, the correction value, and a latency value, the latency value indicating an expected maximum latency time for the air link frame over the wireless channel; and a host interface circuit for receiving and processing the host interface frame based on the host data process signal, and providing the host data to a local host circuit. Nothing in Lockridge discloses this combination of features.

The Examiner asserts that the recited free running timer is shown in Lockridge by the server 202, which receives input signals, which may be in the form of transport packets that include System Clock Recovery (SCR) information, or perhaps by whatever remote element generates the SCR information.

The Examiner asserts that the recited detection circuit is shown in Lockridge by some portion of the server 202 that detects the SCR information, and either the local system clock, which is sampled to generate a counter sample time stamp T2, or perhaps the element that performs the sampling.

The Examiner asserts that the recited wireless transceiver is shown in Lockridge by the Ethernet timestamp board 602. He asserts that since the network may be wireless, it is inherent in the art that any client in the network must have a wireless transceiver and the packet received by the Ethernet timestamp board 602 may include both T1 and T2.

The Examiner asserts that the recited first timestamp processor is shown in Lockridge by the client controller 608, which is responsible for executing a clock recovery algorithm. In particular, the data frame departure times T2 from server 202 are compared to the arrival

times T3 as the client 204. In this manner, the client controller 608 can determine whether a decoder VCXO 812 is faster or slower than a server VCXO 510.

The Examiner asserts that the recited second timestamp processor is also shown in Lockridge by the client controller 608. He asserts that since Applicants disclose only a single time stamp processor in their FIGs. 2 and 6, the recited second time stamp processor is not patentably distinct from the recited first timestamp processor.

The Examiner asserts that the recited host interface circuit is shown in Lockridge by some combination of the client's time stamp board 602, the transport formatter board, the decoder 606, and the client controller 608.

Applicants disagree with numerous assertions and characterizations made by the Examiner in this rejection.

First, Applicants note that claim 22 recites a "receiver device" that comprises the six recited elements. In making this rejection, the Examiner has cited some elements that appear in the server 202 (e.g., to show the recited free running timer and the recited detection circuit), and some elements that appear in the client device 204 (e.g., to show the recited wireless transceiver, the recited first timestamp processor, the recited second timestamp processor, and the recited host interface circuit). But neither the server 202 nor the client device 204 contains all of these elements.

It is impermissible for the Examiner to pick and choose elements from different devices to find every element recited as being in the receiver device in claim 22. And it would also be impermissible for the Examiner to characterize the system 200 as being one large device. FIG. 2 of Lockridge discloses a network system 200 that includes a server 202 that sends data to two client devices 204 and 206. (See, e.g., Lockridge, page 5, line 11,

through page 6, line 16, and FIG. 2.) It would run counter to what is disclosed in Lockridge and what would be understood about Lockridge by one of ordinary skill in the art to consider the network having the server 202 and the client device 204 as being a single receiver device.

Second, claim 22 recites more than just a wireless transceiver that receives first and second time stamps. Claim 22 specifically recites "a wireless transceiver for receiving an air link frame having a host interface packet and a first time stamp, the host interface packet including a second time stamp." Thus, the wireless transceiver must receive both an air link frame and a first time stamp; and the air link frame must itself include a second time stamp. Both limitations are required for Lockridge to properly anticipate this element.

However, nothing in Lockridge discloses that the Ethernet timestamp board 602 receives an air link frame and one of the time stamps T1 and T2, and that the air link frame includes the other of the time stamps T1 and T2.

Third, the Examiner's assertion that the first and second time stamp processors are not patentably distinct simply because only one time stamp processor is shown in the drawings is not correct. Claim 22 recites two separate time stamp processors that perform two separate functions. The first time stamp processor receives the first time stamp and compares the first time stamp with a recorded free-running timing value to determine a timer correction value for the receiver device. The second time stamp processor receives the second time stamp and generates a host data process signal based on the second time stamp, the correction value, and a latency value, the latency value indicating an expected maximum latency time for the air link frame over the wireless channel. Each of these elements includes specific limitations, which must be shown in the cited art if the rejection is to be maintained.

The Examiner has cited the client controller 608 as showing the recited first time stamp processor, and the process of receiving the first time stamp (i.e., T1) and comparing the first time stamp with a recorded free-running timing value to determine a timer correction value for the receiver device. The Examiner has then cited the same client controller 608 as allegedly showing the recited second time stamp processor. But nothing in the cited portion of Lockridge discloses anything regarding the client controller 608 receiving the second time stamp (T2), or generating a host data process signal based on the second time stamp (T2), a correction value, and a latency value. In fact nothing in Lockridge shows anything regarding a latency value that indicates an expected maximum latency time for the air link frame over the wireless channel, nor that any host data process signal is generated based on such a latency value in conjunction with a correction value and the recited second time stamp.

That a single element in the drawings might show the operation of two or more elements in a claim does not make those separate elements patentably indistinct. It merely shows an embodiment in which a single circuit can perform the functions of multiple claim elements. But where those functions are specifically recited, as they are in claim 22, the Examiner must show each of these elements in the cited art in order to prove anticipation. The Examiner has not done so with respect to the recited second time stamp processor.

Therefore, for at least the reasons given above, nothing in Lockridge discloses every feature recited in independent claims 1, 10, 19, and 22. Claims 2-5, 7, and 9 all ultimately depend from claim 1 and are allowable for at least the reasons given above for claim 1; claims 11-14, 16, and 18 all ultimately depend from claim 10 and are allowable for at least the reasons given above for claim 10; claims 20 and 21 depend from claim 19 and are

allowable for at least the reasons given above for claim 19; and claims 23 and 24 depend from claim 22 and are allowable for at least the reasons given above for claim 22.

Therefore, based on at least the reasons given above, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-5, 7, 9-14, 16, and 18-24 under 35 U.S.C. § 102(b) as being allegedly anticipated by Lockridge.

Claim Rejections 35 USC § 103

The Examiner has rejected claims 6 and 15 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Lockridge in view of WIPO publication WO 01/52461 A2 by Tan et al. ("Tan").

Claim 6 depends from claim 1 and is allowable for at least the reasons given above for claim 1; and claim 15 depends from claim 10 and is allowable for at least the reasons given above for claim 10. What Lockridge does not disclose, it likewise does not suggest. And nothing in Tan cures the deficiencies in Lockridge noted above.

Therefore, based on at least the reasons given above, Applicant respectfully requests that the Examiner withdraw the rejection of claims 6 and 15 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Lockridge in view of Tan.

The Examiner has rejected claims 8 and 17 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Lockridge in view of United States Patent No. 5,995,534 to Fullerton ("Fullerton").

Claim 8 depends from claim 1 and is allowable for at least the reasons given above for claim 1; and claim 17 depends from claim 10 and is allowable for at least the reasons given above for claim 10. What Lockridge does not disclose, it likewise does not suggest. And nothing in Fullerton cures the deficiencies in Lockridge noted above.

Therefore, based on at least the reasons given above, Applicant respectfully requests that the Examiner withdraw the rejection of claims 8 and 17 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Lockridge in view of Fullerton.

Conclusion

Applicant respectfully submits that, as described above, the cited prior art does not show or suggest the combination of features recited in the claims. Applicant does not concede that the cited prior art shows any of the elements recited in the claims. However, applicant has provided specific examples of elements in the claims that are clearly not present in the cited prior art.

Applicant strongly emphasizes that one reviewing the prosecution history should not interpret any of the examples Applicant has described herein in connection with distinguishing over the prior art as limiting to those specific features in isolation. Rather, for the sake of simplicity, Applicant has provided examples of why the claims described above are distinguishable over the cited prior art.

In view of the foregoing, Applicant submits that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the Examiner is invited to contact the undersigned by telephone.

Although it is not anticipated that any additional fees are due or payable, the Commissioner is hereby authorized to charge any fees that may be required to Deposit Account No. 50-1147.

Respectfully Submitted,

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Date: 18 November 2008

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